Amendments to the Specification:

Please replace the paragraph beginning at page 12, line 10 with the following amended paragraph:

Figure 7 illustrates the process 700 of decoding variable size instructions and multi-issue instructions from a single register according to one embodiment of the present invention. The process 700 occurs within one clock cycle, and all instructions presented during the process 700 are decoded substantially simultaneously. The process 700 may accept instructions from any of the plurality of sources 505-520. Further, the process 700 may be used even if only a single source is directly connected to the decoder 535. The process 700 begins at a start block 705. Proceeding to block 710, the size and number of instructions are pre-decoded in each of the instruction sources by pre-decoders 707. As stated above, a 64-bit instruction register 507 may include one 64-bit instruction or multiple smaller instructions. For example, the instruction register 507 may include only a 32-bit instruction, a 32-bit instruction in combination with two 16-bit instructions, two 32-bit instructions, or other combinations. The size and number of the instructions may be determined from pre-decoding and the 2-bit width bits. The pre-decoding may be performed in the IF2 pipeline stage, thereby decreasing the burden on the decoder 535. After pre-decoding, the DSP 110 knows how many instructions are in the register and the size of each instruction.